ABSTRACT OF THE DISCLOSURE

A pipeline microprocessor that distributes the instruction dispatching function between a main instruction dispatcher and dispatching logic within a plurality of execution units is disclosed. If the main instruction dispatcher requests load data from a data cache that indicates the data is unavailable, the instruction dispatcher provides to the appropriate execution unit the load instruction (without the load data), a tag (also known by the cache) uniquely identifying the unavailable data, and a false data valid indicator. The cache subsequently obtains the data and outputs it on a bus along with the tag. The dispatching logic in the execution unit is monitoring the bus looking for a valid tag that matches tags of entries in its queue with invalid data indicators. Upon a match, the dispatching logic obtains the data from the bus and subsequently dispatches the instruction along with the data to a functional unit for execution.